

Static Scheduling of Dynamic Execution for High-Level Synthesis

Yuki Toda, Nagisa Ishiura, and Kousuke Sone

This paper presents a concept of *variable* scheduling for high-level synthesis. While the existing schedulers assume fixed delays for all the operations, the latency of memory accesses and serial multiplication/division, for example, may vary depending on operand values. The new scheduling scheme attempts to exploit the dynamic delay variations; the control step to start each operation's execution is dynamically adjusted depending on the completion signals from the preceding operations. Note that the scheduling is adaptive but static, or precomputed during synthesis, thus the hardware would be simpler than that of superscalar microarchitecture. Experimental results show that the number of the execution cycles are reduced by about 4 to 18%, although the sizes of the finite state machines become much larger than that of the conventional fixed scheduling.